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EXAMINER
MOE, AUNG SOE

ART UNIT	PAPER NUMBER
2612	18

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/009,768	KIJIMA ET AL.	
	Examiner	Art Unit	
	Aung S. Moe	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *14-17,19-24 and 38-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *14-17,19-24 and 38-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 14, 16-17, 19-23 and 24 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments filed 7/25/03 have been fully considered but they are not persuasive.

Regarding claims 15 and 24, the Applicant alleged that the Terada reference is not valid prior art under 35 U.S.C. 103 (c) since it only qualifies as prior art under 35 U.S.C. 102(e) and was commonly owned at the time the present invention was made.

In response, the Examiner respectfully disagrees because MPEP 706.02(1)(1) clearly stated that "the amendment to 35 U.S.C. 103(c) **does not affect** any application **filed before November 29, 1999**, a request for examination under 37 CFR 1.129 of such an application, nor a request for continued examination under 37 CFR 1.114 (RCE) of such an application (i.e., see MPEP 706.02(1)(1)." In view of this, it is cleared that the Terada reference is valid prior art under 35 U.S.C. 103 (c) since the instant application was filed on January 20, 1998.

With respect to claims 39-40, the previously elected Species of Figs. 13-17 fails to show the present claimed invention still recited the limitations "c" which recited the features such that "(c) a mode for reading out with **eliminating every third line and summing every line pair** to be read out within the partial imaging area of the imager for use with controlling AF function," thus, the Examiner will maintain the rejection under 35 U.S.C. 112, first paragraph, as set forth as follows:

With respect to the obviousness-type double patenting rejections, although Applicant agrees to file a Terminal Disclaimer (i.e., see page 7 of the remarks) once the later of the two pending applications are in allowable condition, the nonstatutory obviousness-type double patenting rejection will be maintained by the Examiner until a Terminal disclaimer is officially filed.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 14, 16-17, 19, 21-23 and 38-40 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2, 4-21, 24-27, 29-47 and 51 of copending Application No. 08/961,408 in view of Parulski et al. (U.S. 5,828,406) and Whipple et al. (U.S. 5,926,215).

Regarding claims 14, 16-17, 19, 21-23 and 38-40, it is noted that the conflicting claims 1-2, 4-21, 24-27, 29-47 and 51 of copending Application No.08/961,408 are not identical to the claims 14, 16-17, 19, 21-23 and 38-40 of the instant application, they are not patentably distinct from each other because both claimed invention called for an electronic imaging system comprising: a solid-state image sensor (i.e., noted that the optical system, pixel signal output means, and information processing means and trigger means are considered an inherent feature of the electronic imaging system) and control means (i.e., drive control means as claimed in the instant application) for controlling different operation modes, such that a mode for sequentially reading all of the pixel signals for each horizontal line in a vertical direction, a mode for outputting only the electronic pixel signals for n lines per m lines (wherein $m > n$ and $m > 3$), and a mode for causing the solid state imaging device to add adjacent horizontal lines in the vertical direction and output pixel signals corresponding to horizontal lines in the vertical direction as substantially described and connected in the Claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408 and claims 14, 16-17, 19, 21-23 and 38-40 of the instant application.

Furthermore, it is noted that claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408 do not explicitly recite the obviously well-known features as clearly evidenced by Parulski '406 and Whipple '215 as recited in the 103 rejections as discussed below.

In view of this, it would have been obvious to one having ordinary skill in the art at the time invention was made to modify the claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408 as taught by Parulski '406 and Whipple '215 because since such features are well-known in the art for the electronic imaging system to operate different operation modes respectively. In view of this, Claims 14, 16-17, 19, 21-23 and 38-40 of instant application are encompassed by claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408.

This is a provisional obviousness-type double patenting rejection.

5. Claims 15 and 24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408 in view of Terada '888, Parulski '597 and Udagawa '781.

Regarding claims 15 and 24, it is noted that the conflicting claims 1-2, 4-21, 24-27, 29-47 and 51 of copending Application No.08/961,408 are not identical to the claims 15 and 24 of the instant application, they are not patentably distinct from each other because both claimed invention called for an electronic imaging system comprising: a solid-state image sensor (i.e., noted that the optical system, pixel signal output means, and information processing means and trigger means are considered an inherent feature of the electronic imaging system) and control means (i.e., drive control means as claimed in the instant application) for controlling different operation modes, such that a mode for sequentially reading all of the pixel signals for each horizontal line in a vertical direction, a mode for outputting only the electronic pixel signals for n lines per m lines (wherein $m > n$ and $m > 3$), and a mode for causing the solid state imaging

device to add adjacent "q" horizontal lines in the vertical direction and output pixel signals corresponding to horizontal lines in the vertical direction as substantially described and connected in the Claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408 and claims 15 and 24 of the instant application.

Furthermore, it is noted that claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408 do not explicitly recite the obviously well-known features as clearly evidenced by Terada '888, Parulski '597 and Udagawa '781 as recited in the 103 rejections as discussed below. In view of this, it would have been obvious to one having ordinary skill in the art at the time invention was made to modify the claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408 as taught by Terada '888, Parulski '597 and Udagawa '781 because since such features are well-known in the art for the electronic imaging system to operate different operation modes respectively. In view of this, Claims 15 and 24 of instant application are encompassed by claims 1-2, 4-21, 24-27, 29-47 and 51 of copending application 08/961,408.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 39-40 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the

art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 39-40, it is not clear which of the previously elected Species III (i.e., Figs. 13-17) discloses "(c) a mode for reading out with **eliminating every third line and summing every line pair** to be read out within the partial imaging area of the imager for use with controlling AF function," since the elected Species III of Figs. 13-17 merely shows **the summing of first line and third line of the imager** to be read out to control AE, AF and AWB functions.

Therefore, the modes for eliminating every third line and summing (adding) every line pair (i.e., see the limitation "c" of claims 39 and 40) is not described in the elected Species III of Figs. 13-17 in such a way as to enable one skilled in the art to which it pertains.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 14, 16, 17, 19-21 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al. (U.S. 5,668,597) in view of Whipple et al. (U.S. 5,926,215).

Regarding claim 14, Parulski '597 an electronic imaging system (Fig. 1) comprising: a solid-state image sensor (20) having a two-dimensional array of pixels capable of converting light incident thereon to an electric signal (col. 4, lines 15+), the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another (i.e., see Figs. 2A-2B); and

a color filter arranged on an incident plane of the solid-state image sensor (20) having a line sequential primary color mosaic pattern (i.e., see Figs. 2A/2B and 3; noted that the primary color filter of Fig. 3 is the Bayer color filter); and

control means (Fig. 1, the element 27) for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording (col. 6, lines 25+), and

a mode for reading out pixel signal (i.e., noted the focusing mode for providing central lines of image data; see Figs. 4-5 and 10) sums each of n lines ($n \geq 2$, n being an integer) (i.e., noted from the Figs. 4-5 and 10, that the lines 1 and 2 are read out for the auto-focus mode and the read out signals are respectively combined at the output section of the solid-state image sensor 20, thus, the "n" value is equal to two lines; see col. 6, and lines 15+, col. 8, lines 15+) out of every m ($m \geq 3$, m being an integer) lines (i.e., see Fig. 10, the lines 1-4 may be considered as

the 'm' lines) in k ($k \geq 6$, k being an integer) continuous lines of the solid-state image sensor with L ($L > k$) said horizontal lines (i.e., noted that the lines 1-4, 5-8 and 9-n are considered as the 'k' continuous lines which are partial area of the whole sensor lines of "L" as shown in Figs. 4-5, thus, the lines "L" of the whole image sensor is larger than the central area lines "k" as shown in Figs. 4-5 and 10) still picture recording or dynamic image processing (i.e., the still mode/AF mode image processing as discussed in col. 6, lines 15+).

Furthermore, it is noted that although Parulski '597 shows the solid-state image sensor (i.e., Figs. 2A-2B) having a plurality of vertical registers (59) for transferring the pixel signals (58) to the horizontal shift register (70) during the operation of different operation modes (i.e., Still mode & AF mode), Parulski '597 does not explicitly state that the pixel signals are summed by utilizing a plurality of vertical registers as amended in present claimed invention.

However, the above-mentioned claimed limitations are well-known in the art as evidenced by Whipple '215. In particular, Whipple '215 teaches that the pixel signals of n-line of pixel signals read out from the solid-state image sensor (i.e., see Figs. 3 & 5) are summed in the vertical register (36) before they are transferred to the horizontal shift register (38/40) (i.e., noted the BIN as shown in Fig. 5; col. 3, lines 15-20 of Whipple '215).

In view of the above, having the system of Parulski '597 which used the solid-state image sensor with the vertical shift registers (i.e., Fig. 2A of Parulski '597) and then given the well-established teaching of Whipple '215 wherein the charges read from the n-lines are summed in the vertical shift registers (i.e., see col. 3, lines 15-20), it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '597

as taught by Whipple '215, since Whipple '215 states at col. 1, lines 55+ that such a modification would provide a faster frame rate and increase sensitivity while decreasing image memory.

Regarding claim 16, the combination of Parulski '597 and Whipple '215 discloses in which the control means (i.e., Fig. 1, the element's 27 of Parulski '597) controls a mode of reading a plurality of k line blocks each of k lines in the whole lines (i.e., Figs. 4-5 and 10-11 of Parulski '597) for still picture recording or dynamic image processing (i.e., col. 6, lines 15+ and col. 7, lines 10+ of Parulski '597).

Regarding claim 17, the combination of Parulski '597 and Whipple '215 discloses in which image data obtained by reading out pixel signal sums each of n lines (i.e., noted the line 1 and 2 of the Fig. 10 of Parulski '597; see Figs. 5 of Whipple '215) among m vertically continuous lines (i.e., noted the lines 1-4 of Fig. 10 of Parulski '597; Fig. 5 of Whipple '215) for still picture recording or dynamic image processing, is such that its color signal is line sequential data (i.e., Fig. 3, col. 9, lines 5+ and lines 60+ of Parulski '597; Fig. 5 of Whipple '215 teaches that the color signal is line sequential data).

Regarding claims 19 and 20, it is noted that although Parulski '597 shows the use of color filters in which the n addition lines are constituted by the color filter (i.e., see Figs. 6a/6b and 7), and different n line addition filters are provided for every m lines (i.e., the R, G and B filter as shown in Figs. 4 and 7), Parulski '597 does not explicitly state that the n lines for addition are constituted by the same color filter as recited in claims 19 and 20.

However, the above-mentioned claimed limitations are well-known in the art as evidenced by Whipple '215. In particular, Whipple '215 teaches the use of the color filters in the

electronic imaging system wherein the n lines for addition are constituted by the same color filter (i.e., Figs. 3 and 5).

In view of this, having a system of Parulski '597 and then given the well-established teaching of Whipple '215, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '597 as taught by Whipple '215, since Whipple '215 states at col. 2, lines 41+ that such a modification would provide a faster frame rate while preserve the color pixel pattern and effective field of view of the image sensor thereof.

Regarding claim 21, although Parulski '597 shows the use of lines 1-4 as "m" lines, Parulski '597 does not explicitly show wherein m = 2 a +1 ("a" being a positive integer) (i.e., "m" being an odd number) as recited in the present claimed invention. However, Whipple '215 teaches using lines "m" wherein m = 2a +1 ("a" being a positive integer) (i.e., "m" being an odd number) as recited in the present claimed invention (i.e., see Fig. 5 of Whipple '215, noted that lines 7-9 as being an odd number). In view of this, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '597 as taught by Whipple '215, since Whipple '215 states at col. 2, lines 41+ that such a modification would provide a faster frame rate while preserve the color pixel pattern and effective field of view of the image sensor thereof.

Regarding claim 38, noted that claim 38 is rejected for the same reasons as set forth above for claims 14 and 21, please see the Examiner's comments with respect to claims 14 and 21 as discussed above.

11. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski '597 in view of Whipple '215 as applied to claims discussed above, and further in view of Parulski '406 (U.S. 5,828,406).

Regarding claim 22, the combination of Parulski '597 and Whipple '215 discloses the use of AF, AE or AWB control data (i.e., col. 6, lines 15+) by reading a central area of the image sensor (20), however, the combination of Parulski '597 and Whipple '215 does not explicitly show in which **dynamic image processed** signal obtained in either of the above modes is used for AF, AE or AWB control data.

Nevertheless, Parulski '406 teaches that it is conventionally well-known to use a dynamic image processed signal to obtain in "motion" mode and used for AF, AE or AWB control data as recited in present claimed invention (i.e., col. 3, lines 25+, col. 4, lines 30+, col. 9, lines 1-10).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '597 as taught by Parulski '406, since Parulski '406 states at col. 2, lines 41+ that such a modification would provide a relative low quality "motion" mode without increasing the complexity, thereby the operabiiity is improved.

Regarding claim 23, the combination of Parulski '597 and Whipple '215 discloses in which image processed signal obtained in either of the above modes is used as AF, AE or AWB control data (i.e., col. 6, lines 5+), however, the combination of Parulski '597 and Whipple '215 does not explicitly show the use of dynamic image processed signals for AF, AE or AWB control data so that the AF, AE, AWB control data being used to calculated sequentially each in each frame as recited in present claimed invention.

Nevertheless, the above-mentioned claimed limitations are well-known in the art as evidenced by Parulski '406. In particular, Parulski '406 teaches the use of the dynamic image processed signal to obtain AF, AE or AWB control data in either of the still/motion modes, and the AF, AE and AWB control data being calculated sequentially each in each frame (col. 4 lines 10+ and col. 9, lines 1+ of Parulski '406).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '597 as taught by Parulski '406, since Parulski '406 states at col. 2, lines 41+ that such a modification would provide a relative low quality "motion" mode without increasing the complexity, thereby the operability is improved.

12. Claims 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terada et al. (U.S. 6,124,888) in view of Parulski et al. (U.S. 5,668,597) and Udagawa et al. (U.S. 5,880,781).

Regarding claim 15, Terada '888 discloses an electronic imaging system (i.e., see Figs. 7-8 and 10) comprising:

a solid-state image sensor (i.e., Figs. 7/8, the element 103) having a two-dimensional array of pixels capable of converting light incident thereon to an electric signal (i.e., see col. 2, lines 24+ and col. 8, lines 45+), the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another (i.e., see Fig. 8);

a color filter arranged on an incident plane of the solid-state image sensor having a line sequential primary color mosaic pattern (Figs. 27A-28B; ***noted that the use of a color filter is made to Bayer arrangement as disclosed in col. 24, lines 45+***; also see col. 26, lines 40+); and

control means (Figs. 7 and 10; the elements' 109, 108 and 107) for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording (i.e., noted the "whole pixel mode" as shown in Fig. 15; see col. 11, lines 25+ and col. 13, lines 20+),

a mode (i.e., the "skip mode") for reading out pixel signals from some of the lines of the solid-state image sensor for still picture recording or dynamic image processing (i.e., noted the "block mode" as shown in Fig. 15 for motion image processing; see col. 11, lines 25+ and col. 14, lines 35+), and

a mode (i.e., the "block mode") for reading out pixel signals from some of the lines of the solid-state image sensor for still picture recording or dynamic image processing (i.e., noted the "block mode" as shown in Fig. 15 for motion image processing; see col. 11, lines 25+ and col. 13, lines 60+).

Furthermore, it is noted that the third to eight embodiments of Terada '888 does not explicitly state that the "skip mode" is performed by reading out pixel signals sums of n lines among m lines in k ($k \geq 6$, k being an integer) continuous lines of the solid-state image sensor for still picture recording or dynamic image processing.

However, Terada '888 further teaches that the above-mentioned claimed limitations are well-known in the art to modify the imaging system as disclosed in the third to eight embodiments. For example, Terada '888 teaches in the ninth embodiment (i.e., Figs. 25-27B)

that in order to lower substantially the response of the opening and prevent the generation of the return strain (i.e., see col. 24, lines 35+ of Terada '888), it would have been obvious to modify the "skip mode" of the imaging system by reading out pixel signals sums of n lines among **m** lines in **k** ($k \geq 6$, k being an integer) continuous lines of the solid-state image sensor for still picture recording **or** dynamic image processing (i.e., In Figs 27A, it is noted that lines 1 and 3 out of lines 1-3 are added to obtain the line 1 of Fig. 27, and wherein the total of more than 6 output lines may be provided for the motion image processing during the "skip mode"; see col. 26, lines 30+ and col. 28, lines 20+ of Terada '888).

Therefore, having the well-established teaching as discussed in the ninth embodiment of Terada '888, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the "skip mode" of the imaging system as shown in Fig. 7 as suggested in the ninth embodiment of Terada '888, since Terada '888 clearly states at col. 24, lines 36+ that such a modification would lower the response of opening and prevent the generation of the return strain thereof.

Furthermore, with respect to the "block mode", it is noted that although Terada '888 does not explicitly state the particular read out process, such that reading out pixel signal sums each of n ($n \geq 2$, n being an integer) lines among m ($m \geq 3$, m being an integer) lines of the solid-state image sensor, for still picture recording or dynamic image processing, such limitations are also well-known in the art as evidenced by Parulski '597.

In particular, Parulski '597 teaches (i.e., Figs. 1, 4 and 10) that the use of "block mode", wherein pixel signal sums each of n ($n \geq 2$, n being an integer) lines among m ($m \geq 3$, m being an integer) lines of the solid-state image sensor for dynamic image process (i.e., noted that the

sum of each line 1 and 2 among the lines 1-4 of the pixel signals of block "66" may be read out as shown in Figs. 7A/7B and 10/11) so that the block of image signals may be read out for the purposed enabling rapid focus of the imaging system (i.e., see col. 3, lines 25+ and col. 7, lines 4+ of Parulski '597).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Terada '888 as taught by Parulski '597, since Parulski '597 states at col. 3, lines 25+ that such a modification would decrease the required clock rate while enabling rapid focuses of the imaging system thereof.

Furthermore, it is noted that although the combination of Terada '888 and Parulski '597 discloses the solid-state image sensor having a plurality of vertical registers and horizontal shift register (i.e., see col. 2, lines 25+ of Terada '888 and Fig. 2A of Parulski '597) for reading out the pixel signals based on the different modes of operation (i.e., Noted the thin-out read-out modes, such as the block scanning, skip scanning, and whole pixel scanning as shown in Terada '888 and different operation mode such as preview modes, the Central area reading modes for focusing as shown in Figs. 4 and 5 of Parulski '597), the combination of Terada '888 and Parulski '597 does not explicitly state that the read-out pixel signal is summed by utilizing a plurality of vertical registers as amended in the present claimed invention.

However, the above-mentioned claimed limitations are well-known in the art as evidenced by Udagawa '781. In particular, Udagawa '781 teaches that in order to attain a high-speed thin-out reading operation and to obtain high image quality in an electronic imaging system, a color filter array is applied to a solid-state image sensor having a two-dimensional array of pixels (see col. 1, lines 40+) and reading out pixel signal sums of n lines (noted the

elements' C1/M1 as shown in Fig. 2A) out of every m lines (i.e., noted the elements C1, M1, Y2, and G2) within partially continuous k lines (i.e., noted that the pixel signal of C1/M1 and C3/G3 lines are read out for every n lines of multi-pixel CCDs, thus, the value for 'k' is clearly greater than '6' as required by the claimed invention because CCDs having, e.g., 1.6 million pixels; see col. 1, lines 35+ and Fig. 6) of the solid-state image sensor (i.e., Fig. 6) by utilizing a plurality of vertical registers (i.e., the V-CCD; see Figs. 2A-2D and 6; col. 4, lines 30-45).

In view of this, having the combination of Terada '888 and Parulski '597 and then given the well-established teaching of Udagawa '781, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the imaging system of Terada '888 as taught by Udagawa '781, since Udagawa '781 clearly states at col. 2, lines 55+ that such a modification would provide a high-speed thin-out reading operation and high-image quality as obviously desired by the combination of Terada '888 and Parulski '597.

Regarding claim 24, the combination of Terada '888, Parulski '597 and Udagawa '781 discloses in which the control means (Fig. 7, the elements' 108, 106 and 107 of Terada '888) selects a mode of reading out pixel signal sums each of n lines among m vertical continuous lines when obtaining a dynamic image processed signal to be displayed on a display (i.e., the element 106 of Terada '888) provided in it, to be supplied to an external display provided outside it **or** to be used as AE or AWB control data (i.e., see col. 1, lines 45+ of Udagawa '781), and

selects a mode (i.e., see Figs. 7, 10 and 15, the elements' 109, 108 and 107 of Terada '888) of reading out pixel signals of n lines among every m vertically continuous lines in k continuous lines (i.e., col. 28, lines 20+ of Terada '888)when obtaining a dynamic image

processed signal to be used as AF or AE control data (i.e., col. 6, lines 25+ of Parulski '597 and col. 1, lines 45+ of Udagawa '781).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inagaki '634, Watanabe '236, Armstrong 457 and Hosokai '247 discloses an image sensor having different reading modes thereof.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. **Any response to this final action should be mailed to:**
Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or Faxed to:

(703) 872-9314, (for formal communications; please mark "**EXPEDITED PROCEDURE**"; and for informal or draft communications, please label "**PROPOSED**" or "**DRAFT**").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Aung S. Moe** whose telephone number is **(703) 306-3021.** The examiner can normally be reached on Monday-Friday from 9:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wendy Garber**, can be reach on **(703) 305-4929.**

Any inquiry of a general nature or relating to the status of this application should be directed to the customer service number **(703) 306-0377.**

AUNG MOE
PRIMARY EXAMINER

A. Moe

September 25, 2003